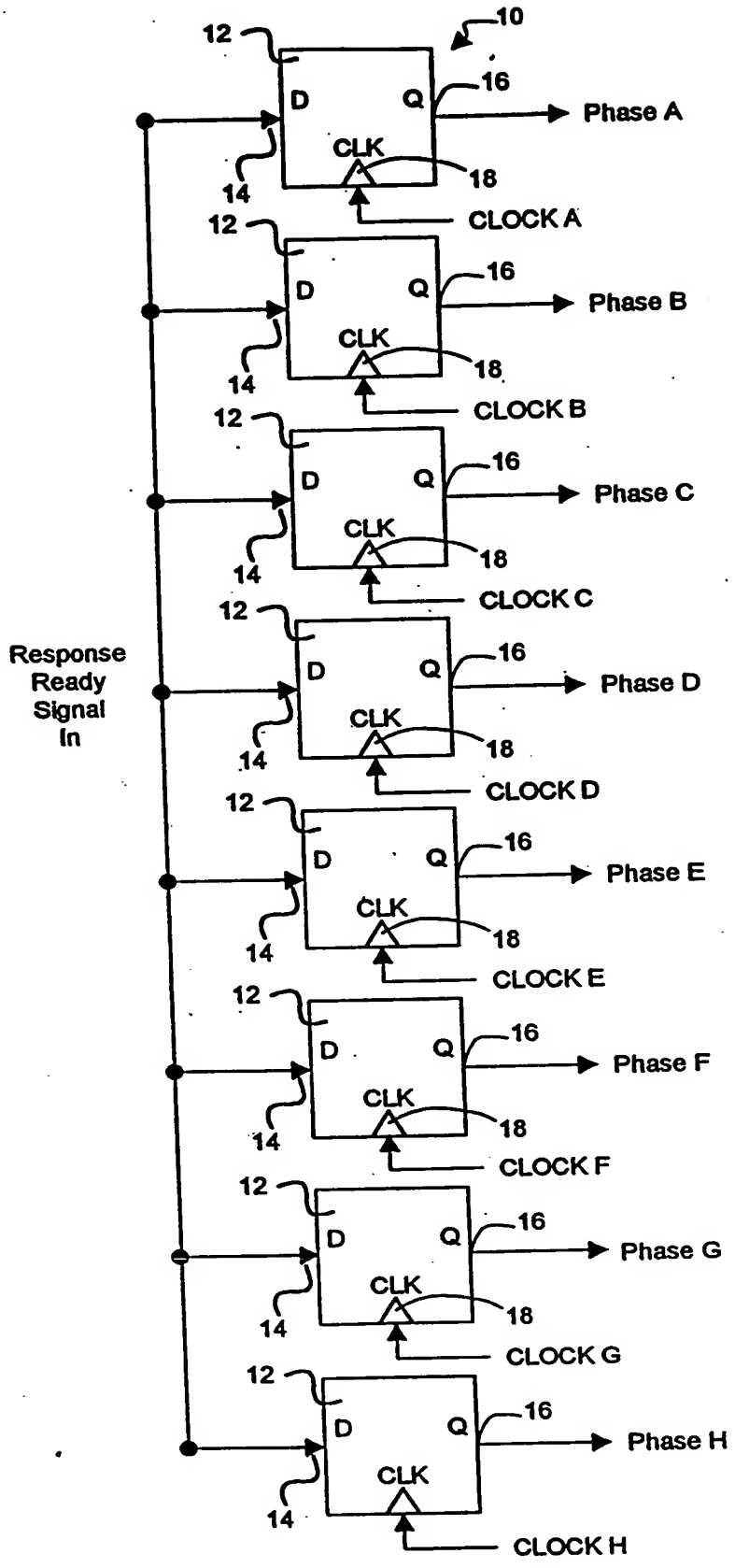

Figur 1 - Signal Transition Phas D tector

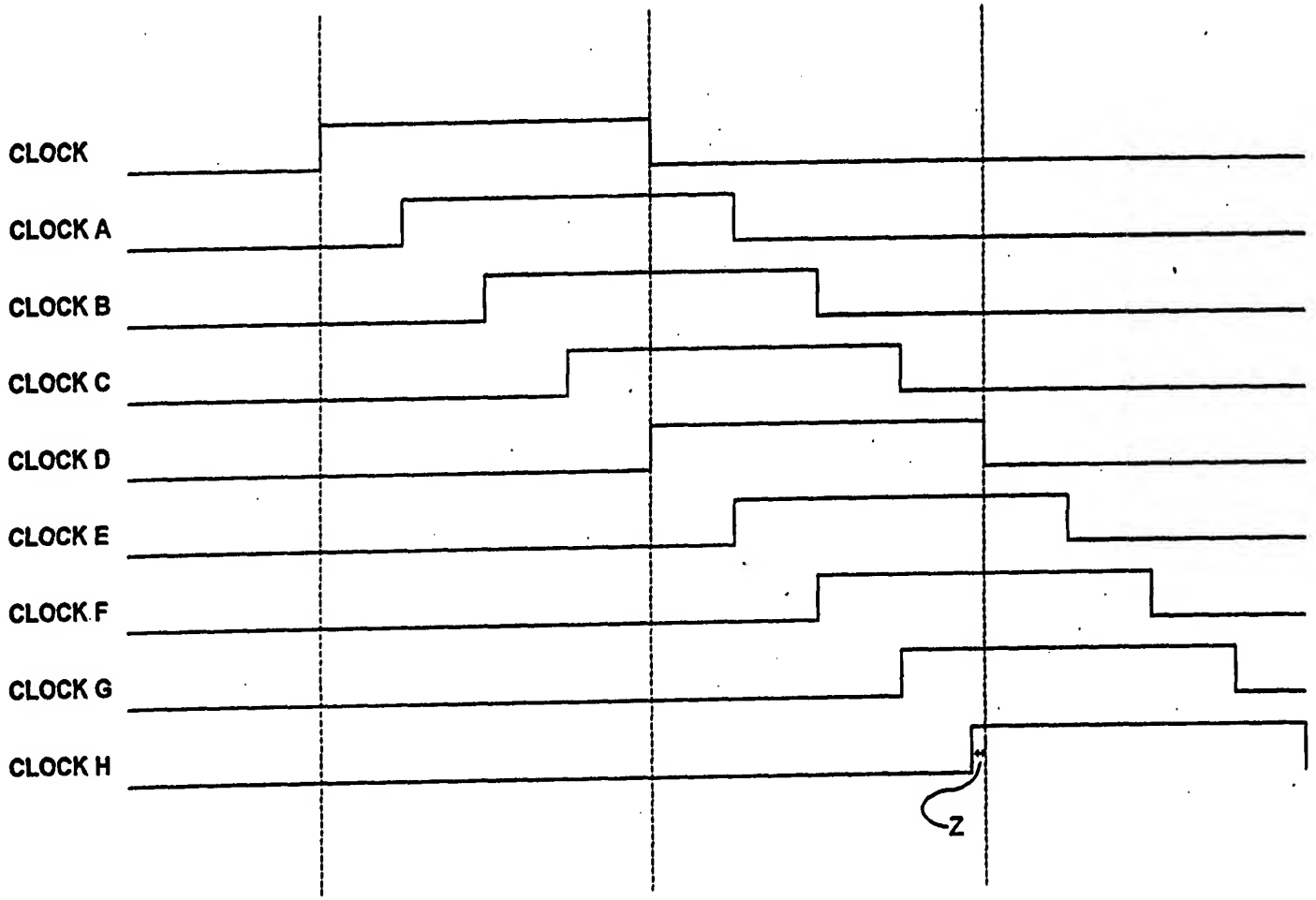

Figure 2 - Clock Timing Diagram

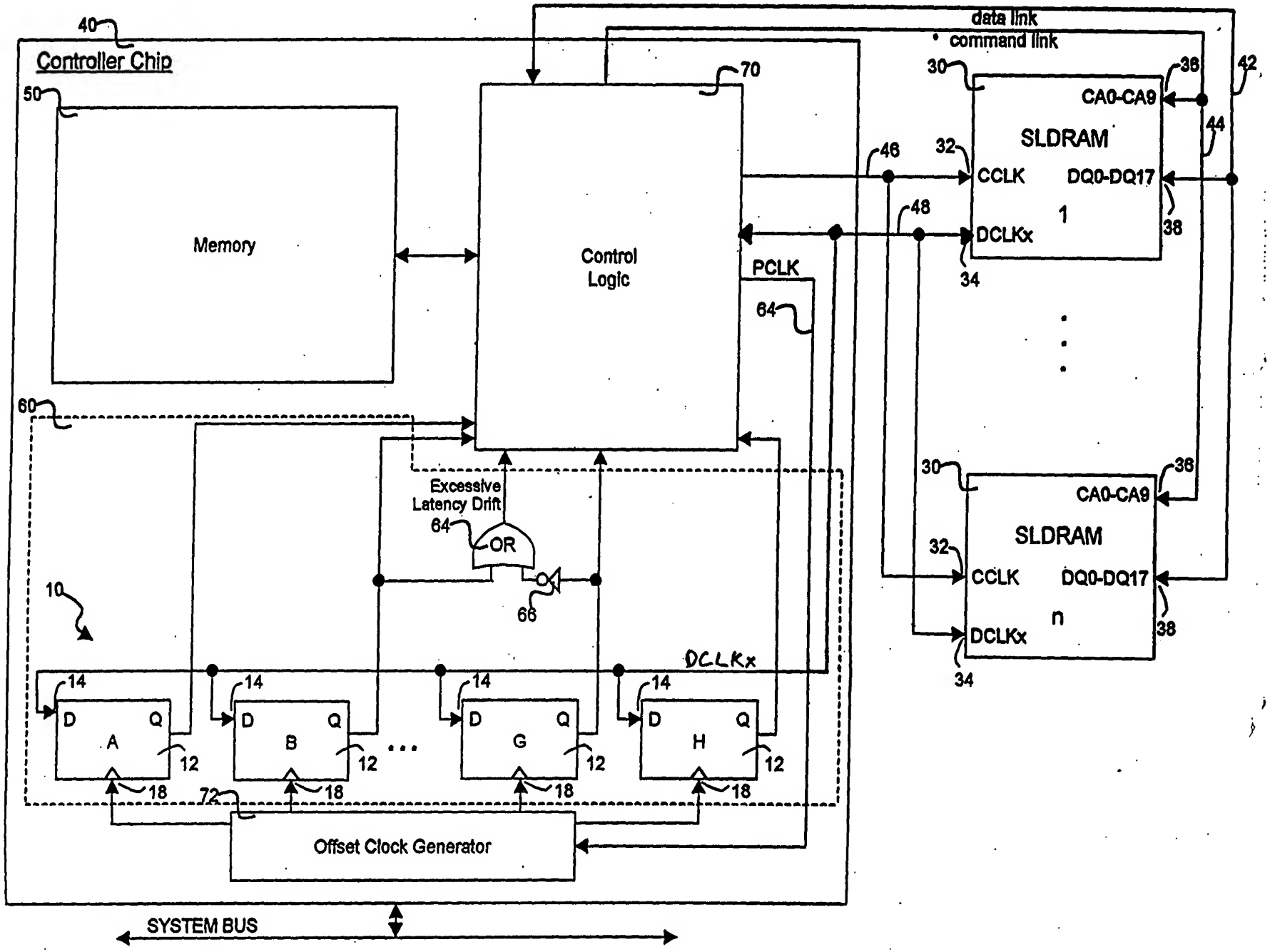
40
Controller Chip
50
Memory
70
Control Logic
data link
command link
30
CA0-CA9
SLDRAM
32
CCLK
DQ0-DQ17
1
DCLKx
34
36
38
42
44
46
48
PCLK
64
60
Excessive Latency Drift
OR
66
10
DCLKx
14
D
Q
A
B
G
H
12
18
72
Offset Clock Generator
SYSTEM BUS
n

Figure 3

READ AND WRITE COMMAND PACKET DEFINITION

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	BNK2	BNK1	BNK0	ROW9	ROW8
0	ROW7	ROW6	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0	0	0
0	0	0	0	COL6	COL5	COL4	COL3	COL2	COL1	COL0

Legend:

ID8-ID0 = Device ID Value
CMD5-CMD0 = Command Code
BNK2-BNK0 = Bank Address.
x = don't care

ROW9-ROW0 = Row Address
COL6-COL0 = Column Address
0=Unused, apply 0 for this bit

Figure 4

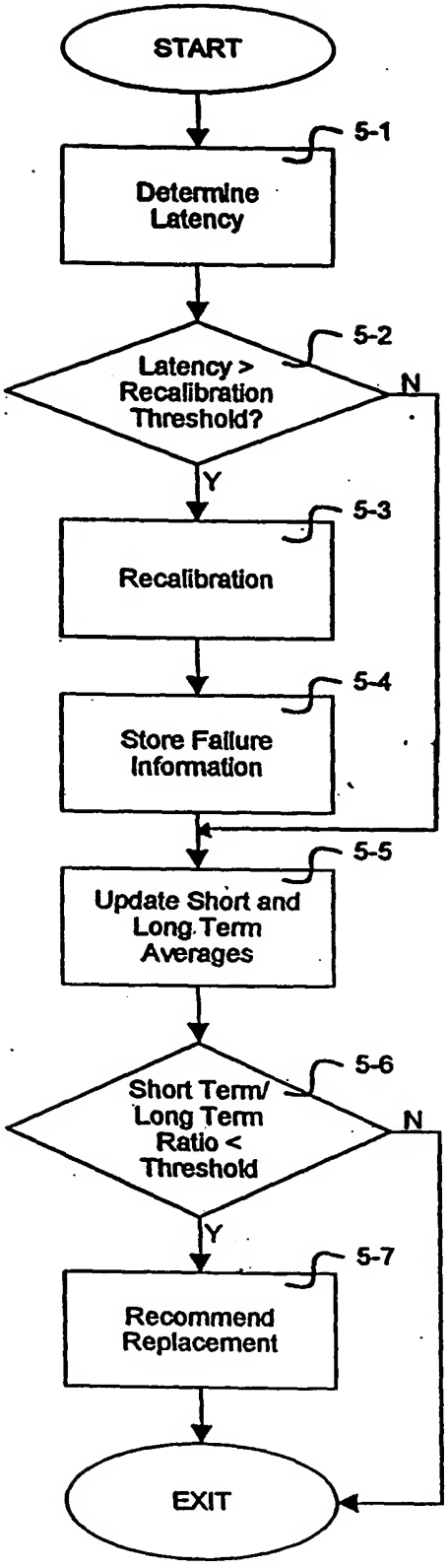
START
5-1
Determine Latency
5-2
Latency > Recalibration Threshold?
N
Y
5-3
Recalibration
5-4
Store Failure Information
5-5
Update Short and Long Term Averages
5-6
Short Term/ Long Term Ratio < Threshold
N
Y
5-7
Recommend Replacement
EXIT

Figure 5

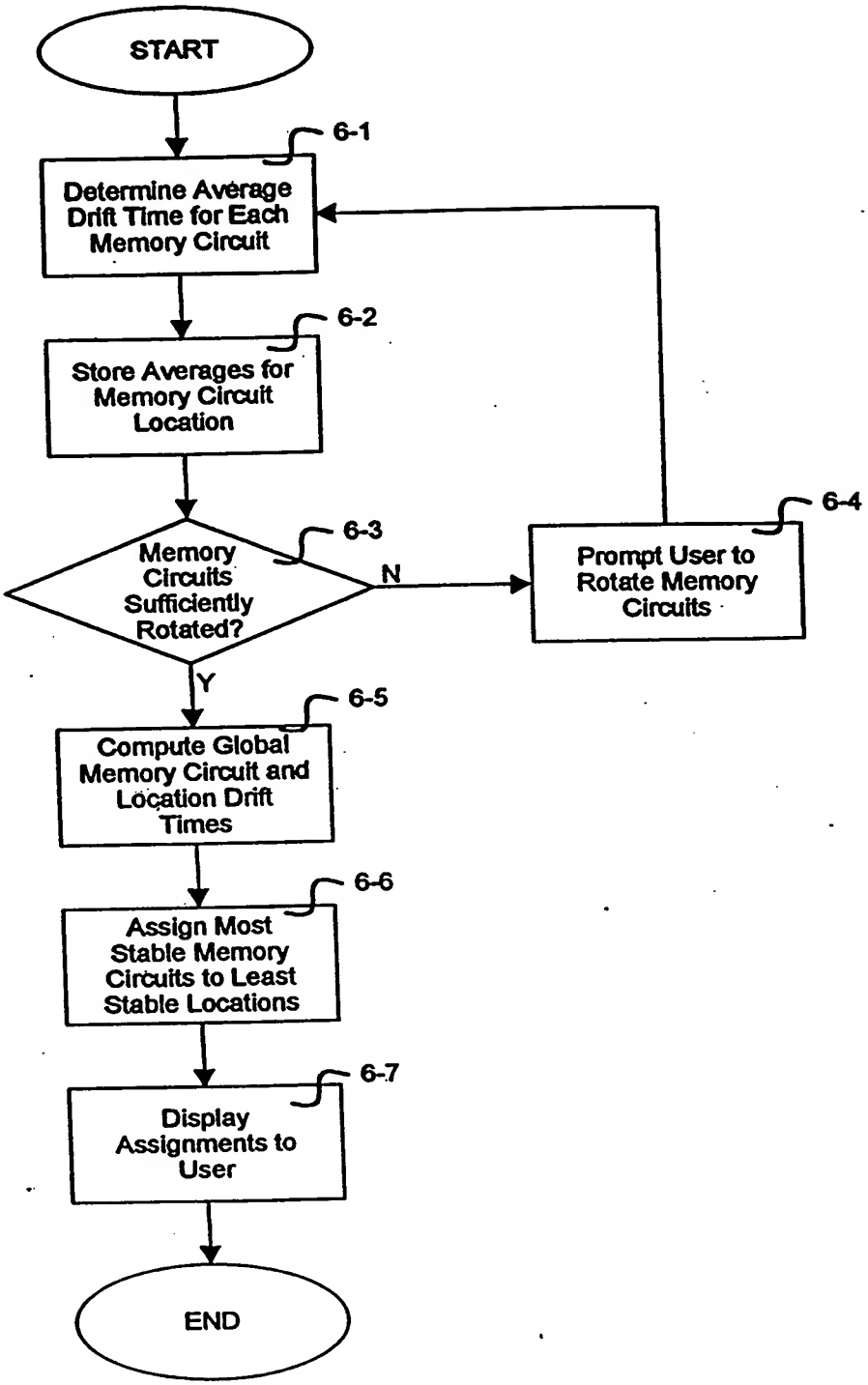
START
6-1
Determine Average Drift Time for Each Memory Circuit
6-2
Store Averages for Memory Circuit Location
6-3
Memory Circuits Sufficiently Rotated?
N
6-4
Prompt User to Rotate Memory Circuits
Y
6-5
Compute Global Memory Circuit and Location Drift Times
6-6
Assign Most Stable Memory Circuits to Least Stable Locations
6-7
Display Assignments to User
END

Figure 6

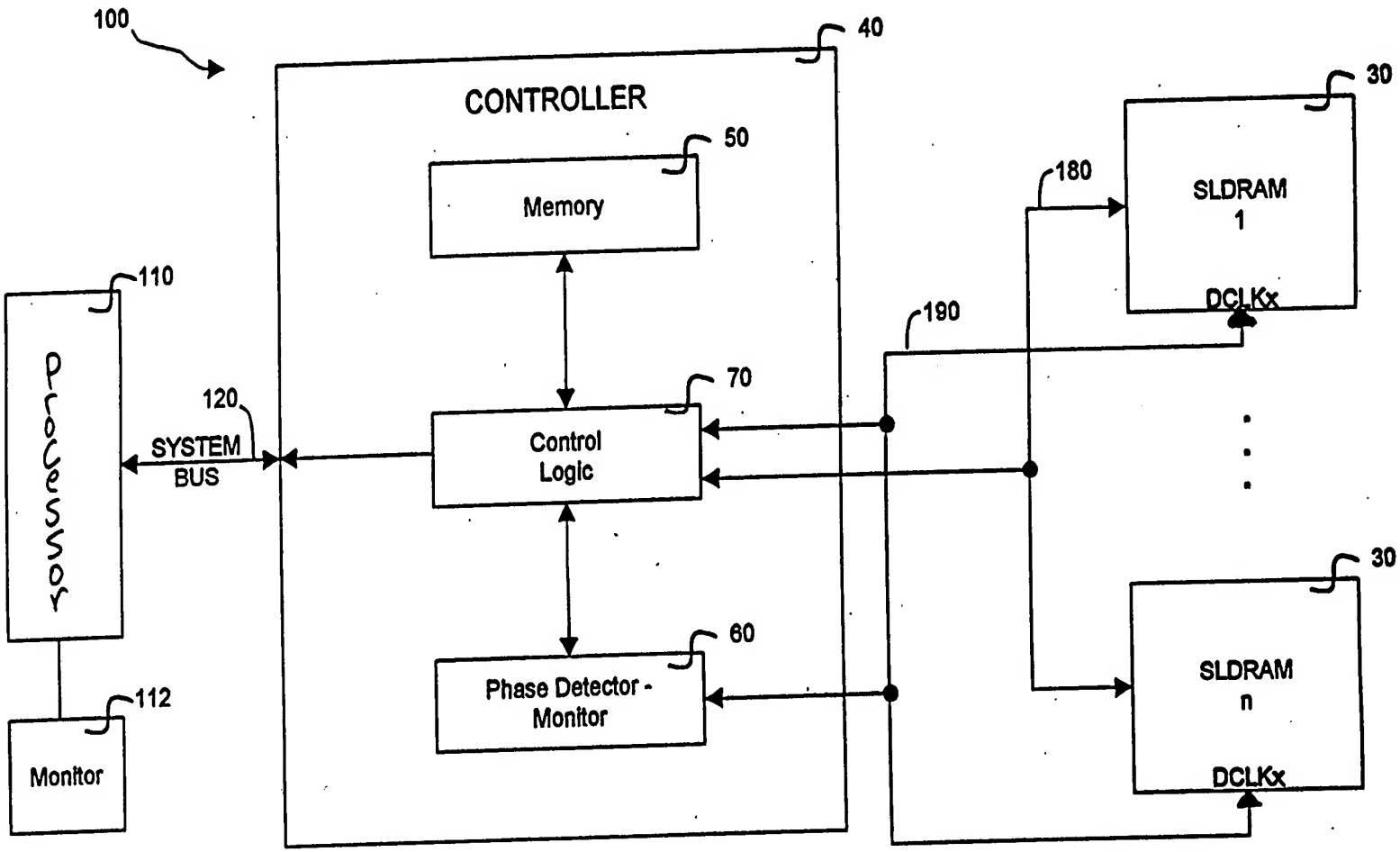
100
40
CONTROLLER
50
Memory
30
180
SLDRAM
1
DCLKx
110
Processor
120
SYSTEM
BUS
190
70
Control
Logic
30
60
Phase Detector -
Monitor
SLDRAM
n
DCLKx
112
Monitor

Figure 7